(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 660 396 A1**

(12) # EUROPEAN PATENT APPLICATION

(21) Application number: 93830523.2

(22) Date of filing: 24.12.93

(51) Int. Cl.6: H01L 23/051, H01L 23/48

(43) Date of publication of application: 28.06.95 Bulletin 95/26

(84) Designated Contracting States: DE FR GB IT

(71) Applicant: CONSORZIO PER LA RICERCA SULLA MICROELETTRONICA NEL MEZZOGIORNO
Stradale Primosole, 50
I-95121 Catania (IT)

(72) Inventor: Ronsisvalle, Cesare
Via Argo, 22
I-95126 Catania (IT)

(74) Representative: Mittler, Enrico et al
c/o Marchi & Mittler s.r.l.
Viale Lombardia, 20
I-20131 Milano (IT)

(54) **Power MOS device chip and package assembly.**

(57) In a power MOS device chip and package assembly, the package comprises a thermally conducting body (21) and an electrically conducting contact washer (16) pressed to be in close mechanical contact with a top surface of the chip (22) and with an external electrical terminal (12), the top surface of the chip being represented by a metal layer (10) covering a conductive material gate layer (8) of the power MOS device; the chip (22) comprises a plurality of functionally inactive regions (11) whereover the gate layer (8) and the metal layer (10) are elevated with respect to the remaining of the chip (22), so that the pressure exerted by the contact washer (16) is entirely sustained by said at least one functionally inactive regions (11).

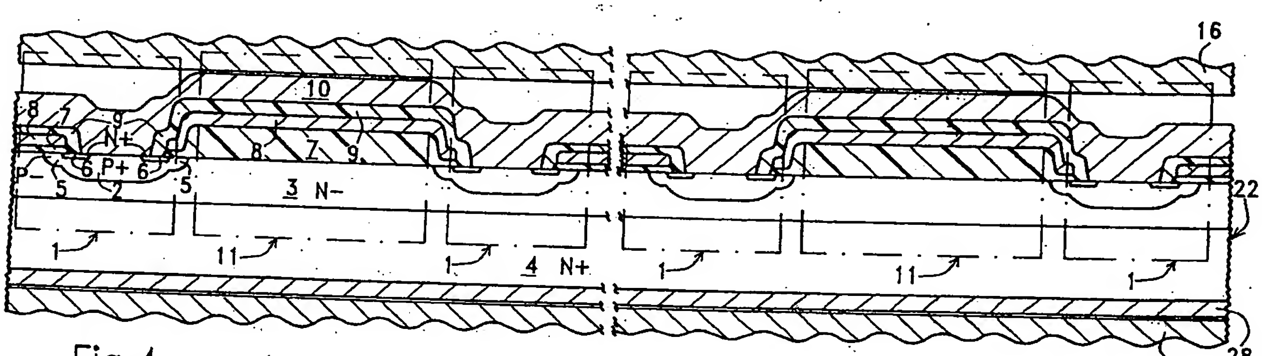

Fig.4

The present invention relates to a power MOS device chip and package assembly.

Power semiconductor devices having large chip size, with a chip diameter larger than 2 or 3 cm, are generally packaged in ceramic packages, such as the so-called "press-pack" package, which, differently from plastic packages, guarantee a higher degree of heat dissipation.

Due to the high power managed by the semiconductor device, the contact area between the device chip and the external leads (normally constituted by nickel-plated copper) must be as wide as possible; this makes the use of wire bonding techniques, commonly used for power devices with lower power ratings packaged in plastic or metallic packages, impracticable; the leads are therefore electrically connected to the chip by means of molybdenum or tungsten plates which at one side are in physical contact with the leads, while at the other side are in electrical contact with the chip through thin washers or discs of silver or silver-plated copper.

To achieve a good electrical contact, and thus to reduce the contact resistance, the contact pressure between the leads, the plates, the washers or the discs and the chip must be rather high.

This technique is efficiently used in connection with semiconductor devices such as diodes, silicon controlled rectifiers (SCRs), gate turn-off thyristors (GTOs), triacs and so on, but its application to MOS power devices (power MOSFETs, IGBTs, MCTs, etc.) poses some problems: since in fact such devices are characterized by having fragile oxide and polysilicon layers at their surface, the contact pressures required to achieve good electrical contact would cause such layers to be damaged.

It is however known that power MOS devices are expected to replace the more common thyristors even in the high-power field.

In view of the state of the art described, object of the present invention is to realize a power MOS device chip and package assembly which is not affected by the abovementioned drawbacks, while assuring good heat dissipation characteristics and low contact resistance.

According to the present invention, such object is attained by means of a power MOS device chip and package assembly, the package comprising a thermally conducting body and an electrically conducting contact washer pressed to be in close mechanical contact with a top surface of the chip and with an external electrical terminal, said top surface of the chip being represented by a metal layer covering a conductive material gate layer of the power MOS device, characterized in that the chip comprises a plurality of functionally inactive regions whereover the gate layer and the metal layer are elevated with respect to the remaining of the chip, so that the pressure exerted by the contact washer is entirely sustained by said functionally inactive regions.

Thanks to the present invention, it is possible to realize power MOS devices which can be packaged using the same techinque used for traditional power semiconductor devices which are not affected by problems related to fragile surface structures.

The features of the present invention will be made more evident by the following detailed description of one embodiment, illustrated as a non-limiting examples in the annexed drawings, wherein:

Figure 1 is an exploded perspective view of a power MOS device chip and package assembly according to the invention;

Figure 2 is a cross-sectional view of the assembly of Figure 1;

Figure 3 is a schematic top plan view of a part of the power MOS device chip of Figure 1;

Figure 4 is a cross-sectional view taken along the plane IV-IV of Figure 3.

A so-called "press-pack" ceramic package, shown in Figures 1 and 2 and described for example in the European Patent Application No. 91830215.9 filed on May 23, 1991, for a power semiconductor device chip 22 comprises a first pair of plates 12 and 13 of nickel-plated copper, constituting two external electrodes of the power device packaged therein, a second pair of plates 14 and 15 of molybdenum, a contact washer 16 of silver-plated copper or silver or molybdenum, a contact disc 17 also of silver-plated copper or silver or molybdenum, an upper flange 18, an intermediate flange 19 and a lower flange 20 all in nickel-plated copper, and a ceramic body 21. The power device chip 22 is interposed between the contact washer 16 and the contact disc 17, and is kept in position by a plastic washer 23 (Fig. 2). The ceramic body 21 is provided with a passing-through hole 24 for a metallic wire 25 supplying a control signal for the power device, the metallic wire 25 ending with a spring-shaped end 26; the passing-through hole 24 is externally connected to a terminal 27.

In Figure 3 a top view of a part of the chip 22 is shown. A power MOS device, for example a power MOSFET, is composed in a per-se known way by a plurality of functionally active elementary cells 1, also called "source cells", disposed to form a bidimensional array. As shown in Figure 4, the chip 22 comprises an N+ semiconductor substrate 4 over which an N-epitaxial layer 3 is grown. Each source cell 1 represents a functionally active unit of the whole power MOSFET, and contributes by a respective fraction to the overall power MOSFET

current capability. Each source cell 1 comprises a P+ deep body region 2 obtained into the N- epitaxial layer 3. The P+ deep body region 2 is laterally surrounded by and merged with a P- annular region 5 constituting a channel region of the source cell 1; inside the P type semiconductor region composed by the P- annular region 5 and by the P+ deep body region 2, an N+ annular region 6 is obtained constituting a source region of the elementary source cell 1. At a top surface of the N-epitaxial layer 3, an oxide layer 7 having a typical thickness of about 0.85 μm extends over the P- annular region 5 and partially over the N+ annular region 6 and constitutes a gate oxide layer of the source cell 1; a polysilicon layer 8 is superimposed over and autoaligned with the underlying oxide layer 7, and constitutes a polysilicon gate layer of the source cell 1. An insulating layer 9 covers the polysilicon layer 8 and is selectively etched to form contact areas to allow an overlying metal layer 10 to come into contact with both the N+ annular region 6 and the P+ deep body region 2; the metal layer 10 contacts in the same way all the elementary source cells 1 and constitutes a source electrode for the power MOSFET. A bottom surface of the N+ substrate 4 is covered by a metal layer 28 constituting a drain electrode for the power MOSFET. A contact area for the polysilicon gate layer 8 is also provided at the top surface of the chip 22, even if not shown in the drawings, to allow the spring-shaped end 26 of the wire 25 to electrically contact the polysilicon gate layer 8 when the chip 22 is packaged in the "press-pack" package described above.

According to the present invention, the bidimensional array of source cells 1 includes dummy cells 11, which are inactive from the functionally point of view and do not contribute to the overall current capability of the power MOSFET.

In the example of Figure 3 such dummy cells 11 are disposed to form a grid with lines of dummy cells 11 regularly spaced in both the horizontal dimensions by an equal number of source cells 1. The dummy cells 11 have horizontal dimensions substantially identical to those of the source cells 1, but different vertical dimension. This clearly appears in Figure 4, wherein the cross-section of two of such dummy cells 11 is shown.

Differently from the elementary source cells 1, no P+ deep body region 2, P- annular region 5 and N+ annular region 6 are provided in the dummy cell 11; furthermore, the thickness of the oxide layer 7, typically of 2 μm, is greater than the thickness of said oxide layer 7 in the source cells 1: this causes the surface of the metal layer 10 to be elevated over the dummy cells 11 with respect to the source cells 1.

When the chip 22 is to be packaged into the press-pack package described above, the chip 22 is inserted into the ceramic body 21 so that the metal layer 28 leans on the contact disc 17, which in turn leans on the plate 15. The bottom of the body 21 is closed by the lower flange 20 and by the plate 13. The contact washer 16 is then deposited over the top surface of the chip 22, i.e. over the metal layer 10. The top of the body 21 is closed by the plate 26 and by the upper flange 18. To achieve a good electrical contact, the plate 12 is pressed down to put the washer 16 into close mechanical contact with the top surface of the chip 22.

Thanks to the fact that the metal layer 10 protrudes superiorly over the dummy cells 11 with respect to the source cells 1, the contact washer 16 leans on the dummy cells 11 and not on the source cells 1; the contact pressure is thus entirely sustained by the dummy cells 11 which, because of the greater thickness of the oxide layer 7, are more resistant to mechanical stresses than the source cells 1. It is thus possible to obtain a good electrical contact without damaging the power MOSFET.

Various topological distribution of dummy cells 11 and elementary source cells 1 are possibile, depending on the contact pressure, i.e. on the contact resistance, requested.

Claims

1. Power MOS device chip and package assembly, the package comprising a thermally conducting body (21) and an electrically conducting contact washer (16) pressed to be in close mechanical contact with a top surface of the chip (22) and with an external electrical terminal (12), said top surface of the chip being represented by a metal layer (10) covering a conductive material gate layer (8) of the power MOS device, characterized in that the chip (22) comprises a plurality of functionally inactive regions (11) whereover the gate layer (8) and the metal layer (10) are elevated with respect to the remaining of the chip (22), so that the pressure exerted by the contact washer (16) is entirely sustained by said functionally inactive regions (11).

2. Power MOS device chip and package assembly according to claim 1, the power MOS device being composed by a plurality of functionally active elementary cells (1) obtained in respective portions of the chip (22), characterized in that said functionally inactive regions (11) are intercalated to the functionally active elementary cells (1), and the gate layer (8) and

the metal layer (10) over the functionally inactive regions (11) are elevated with respect to the functionally active elementary cells (1).

3. Power MOS device chip and package assembly according to claim 2, characterized in that the conductive material gate layer (8) is insulated from an underlying semiconductor material (3) by an insulation layer (7) which is thicker in the functionally inactive regions (11) than in the functionally active elementary cells (1), to cause the gate layer (8) and the metal layer (10) to be elevated over the functionally inactive regions (11) with respect to the functionally active elementary cells (1).

4. Power MOS device chip and package assembly according to anyone of the preceding claims, characterized in that said thermally conducting body (21) of the package is made of ceramic.

5. Power MOS device chip and package assembly according to claim 4, characterized in that the package is of the "press-pack" type, the ceramic body (21) containing the chip (22), the contact washer (16) in contact with the top surface of the chip, an electrically conducting contact disc (17) in mechanical contact with a bottom surface (28) of the chip (22), a first electrically conducting plate (14) superimposed over the contact washer (16), a second electrically conducting plate (15) underlying the contact disc (17), the package further comprising an upper flange (18) closing a top opening of the body (21) and a lower flange (20) closing a bottom opening of the body (21), and two external plates (12,13) in contact with a respective one of said two flanges (18,20) and constituting external electrical terminal of the power MOS device.

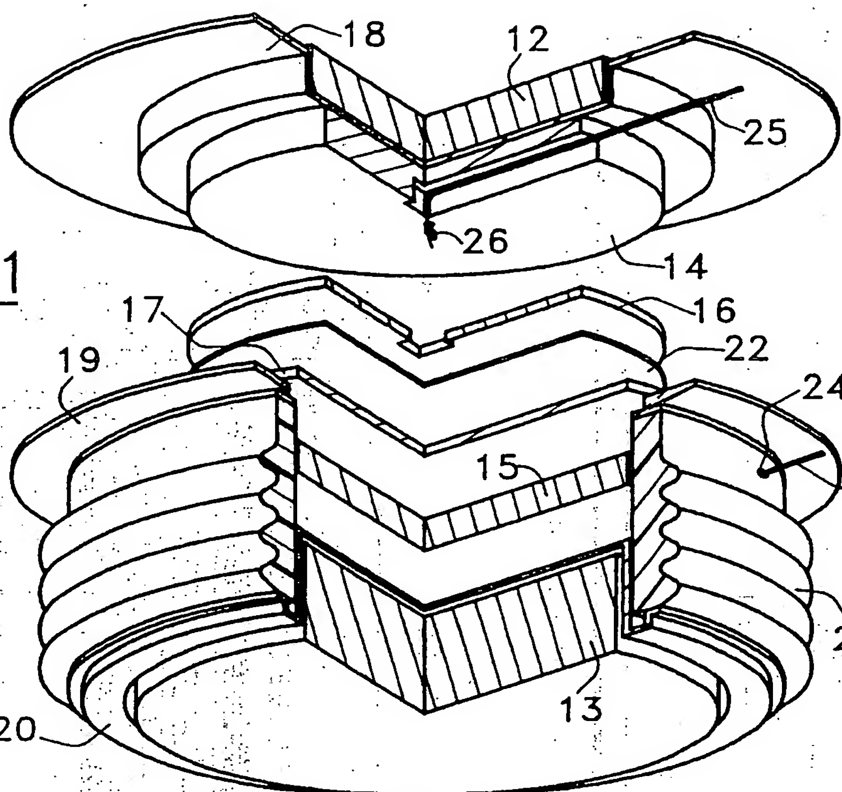
18
12
25
26
14
17
16
19
22
24
27
15
21
20
13

Fig. 1

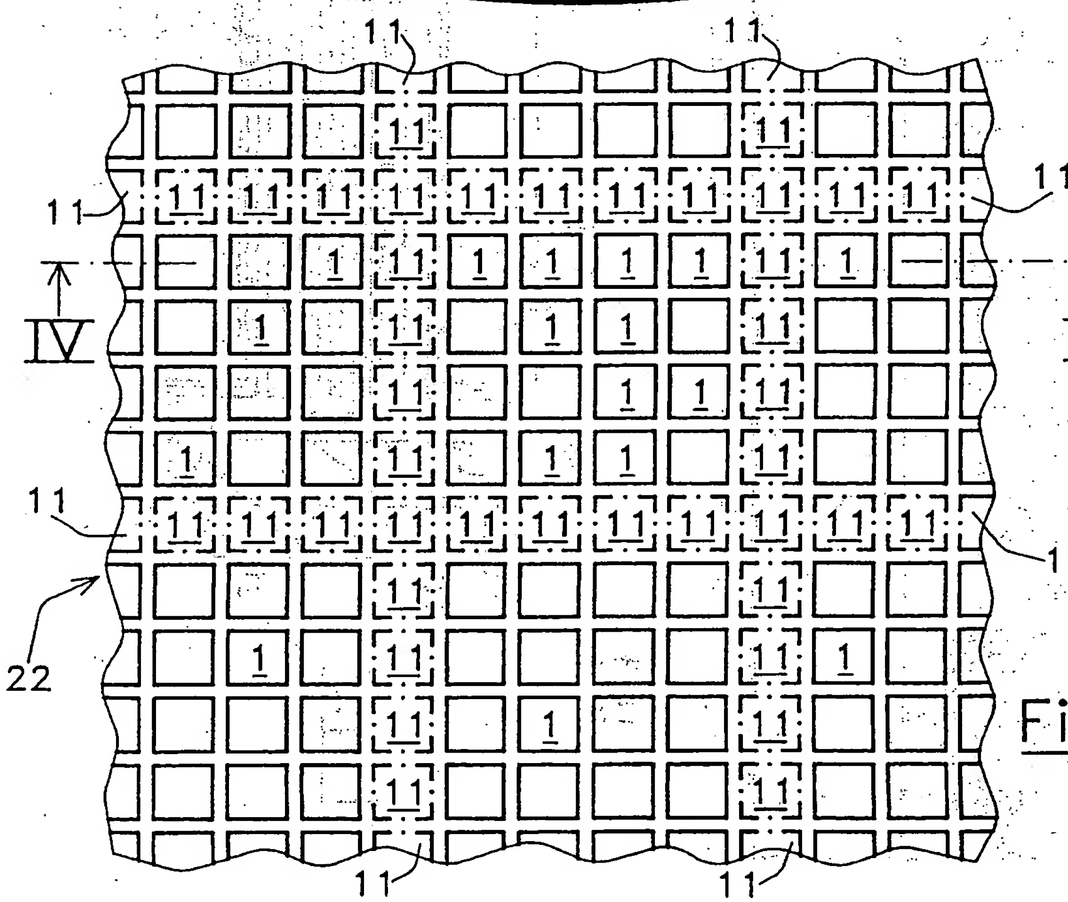
11
11
11
11
11
11
IV
IV
1
22
11
11

Fig. 3

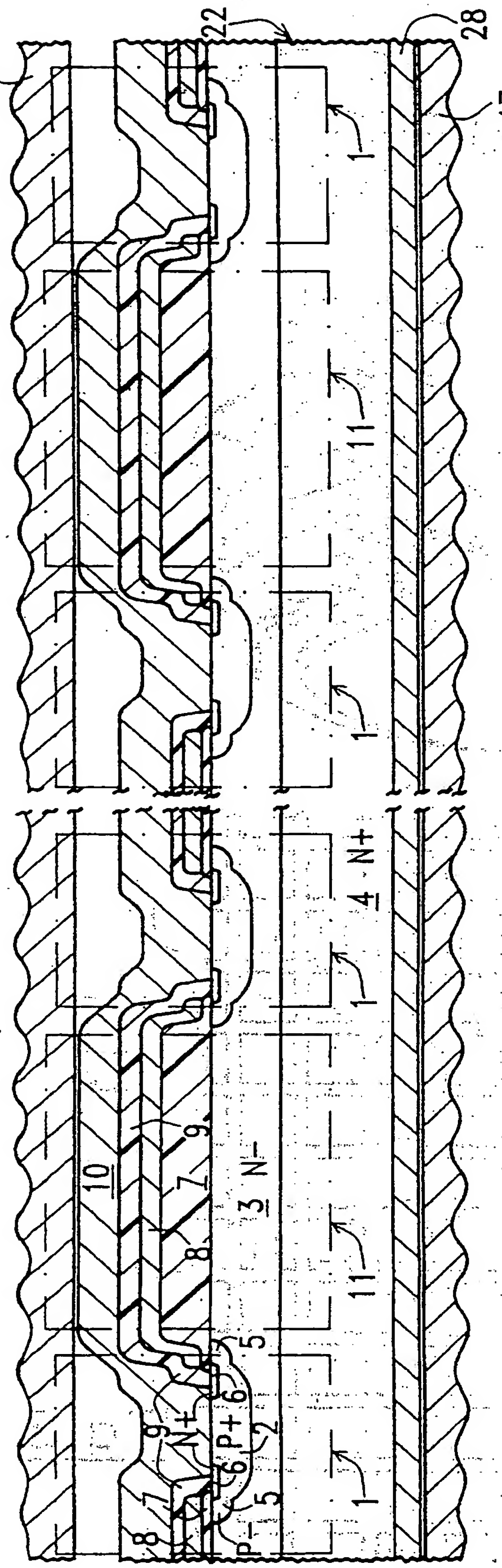

Fig.4

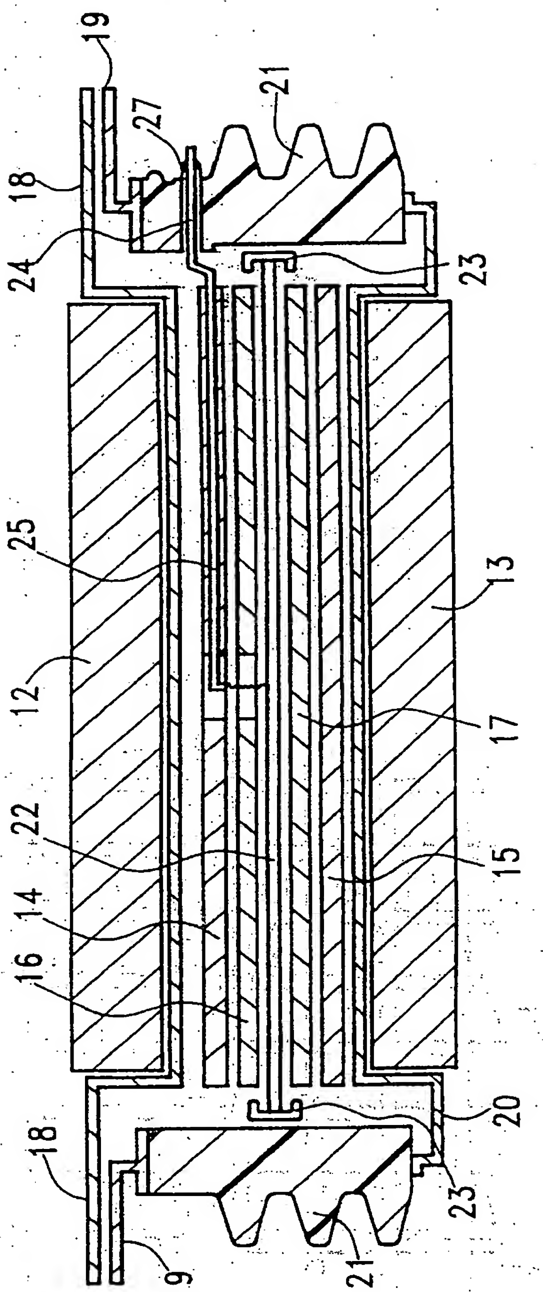

Fig.2

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 83 0523

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP-A-0 433 650 (TOSHIBA) * column 16, line 11 - line 14; claims 1,4; figures 1,5,23 *	1-3	H01L23/051 H01L23/48
A	EP-A-0 421 344 (TOSHIBA) * column 9, line 17 - line 21; claim 1; figure 1 *	1,4,5	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	15 April 1994	De Raeve, R

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)